ABSTRACT

A method of forming a double-gated transistor comprising the following steps. A substrate having an SOI structure formed thereover is provided. The SOI structure including a lower SOI oxide layer and an upper SOI silicon layer. A top oxide layer is formed over the SOI structure. A first top dummy layer is formed over the top oxide layer. The first top dummy layer, top oxide layer, and upper SOI silicon layer are patterned to form a patterned first top dummy layer/top oxide layer/upper SOI silicon layer stack having exposed side walls. The patterned upper SOI silicon layer including a source region and a drain region connected by a channel portion. A rounded oxide layer is formed over the exposed side walls of the patterned upper SOI silicon layer which also rounds the patterned upper SOI silicon layer. The patterned first top dummy layer is removed, exposing the patterned top oxide layer. A second patterned dummy layer is formed over the exposed patterned top oxide layer and the exposed portions of the upper SOI silicon layer. The second patterned dummy layer having an opening that defines a gate area exposing: a portion of the oxide layer within the gate area; portions of the upper surface of the lower SOI oxide layer within the gate area; and a portion of the rounded oxide layer within the gate area. The exposed gate area portions of the upper surface of the lower SOI oxide layer are etched into the lower SOI oxide layer to: form an undercut into the undercut lower SOI oxide layer exposing a bottom portion of the patterned upper SOI silicon layer within the gate area; remove the exposed gate area portion of the oxide layer exposing a top portion of the patterned upper SOI silicon layer within the gate area; and remove the portion of the rounded oxide layer within the gate area exposing a portion of the side walls of the patterned upper SOI silicon layer within the gate area. A conformal oxide layer is

formed over: the exposed bottom portion of the patterned upper SOI silicon layer within the gate area; the exposed top portion of the patterned upper SOI silicon layer within the gate area; and the exposed portion of the side walls of the patterned upper SOI silicon layer within the gate area. A gate is formed within the second patterned dummy layer opening and includes an upper gate above the patterned upper SOI silicon layer within the gate area and a lower gate under the upper SOI silicon layer within the gate area. The second patterned dummy layer is removed to form the double-gated transistor.